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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/662,228	09/14/2000	Peter N. Ehlig	TI-14081.3A2	3050

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Lawrence J Bassuk
Texas Instruments Incorporated
Mail Station 3999
P O Box 655474
Dallas, TX 75251

EXAMINER

OPIE, GEORGE L

ART UNIT	PAPER NUMBER
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2126

DATE MAILED: 05/19/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

Applicant(s)

09/662,228

Ehlig et al.

Examiner

Art Unit

George L. Opie

2151

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

- 1) ☒ Responsive to communication(s) filed on 27 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 41-51 is/are pending in the application.
- 4a) Of the above claim(s) ☐ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ☐ is/are allowed.
- 6) ☒ Claim(s) 41-51 is/are rejected.
- 7) ☐ Claim(s) ☐ is/are objected to.
- 8) ☐ Claim(s) ☐ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ☐ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on ☐ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- a) ☐ All b) ☐ Some * c) ☐ None of the CERTIFIED copies of the priority documents have been:
1. ☐ received.
2. ☐ received in Application No. (Series Code / Serial Number) ☐.
3. ☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. 119(e).

Attachment(s)

- 14) ☒ Notice of References Cited (PTO-892)
- 15) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 16) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ☐
- 17) ☐ Interview Summary (PTO-413) Paper No(s). ☐
- 18) ☐ Notice of Informal Patent Application (PTO-152)
- 19) ☒ Other: Text docs for USP4,554,413 USP4,484,274

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DETAILED ACTION

This Action is responsive to Amendment A, filed 27 February 2004, in which claims 1-40 were cancelled, and new claims 41-51 were added for examination.

1. Request for copy of Applicant's response on floppy disk:

Please help expedite the prosecution of this application by including, along with your amendment response in paper form, an electronic file copy in WordPerfect, Microsoft Word, or in ASCII text format on a 3½ inch IBM format floppy disk.

Please include all pending claims along with your responsive remarks. Only the paper copy will be entered -- your floppy disk file will be considered a duplicate copy. Signatures are not required on the disk copy. The floppy disk copy is not mandatory, however, it will help expedite the processing of your application. Your cooperation is appreciated.

2. **Obviousness-type double patenting rejection**

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. CIT. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Uogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

"Double patenting rejection of application claims was fully justified where applicant, in course of expanding first application to disclose enough more by way of details, alternatives, and additional uses to support broad, dominating, generic claims in later applications, has disclosed no additional invention or discovery other than that what was already claimed in patent on first application; there is significant difference between justifying broadening of claims and disclosing additional inventions." *In re Van Ornum*, 214 USPQ (CCPA 1982).

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Claims 41-51 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-11 of application 08/617,673 filed May 2, 1996, now U.S. Patent 6,134,578.

Although the conflicting claims are not identical, they are not patentably distinct from each other because of corresponding language that recites many of the same elements and functions claimed in the previously patented invention, i.e., *"a semiconductor chip", "a processor formed on the chip", "the processor including an ALU and selected registers that are associated with the ALU, each selected register being formed of a pair of first and second registers, the ALU storing program data in one of the first and second registers for each selected register" "a context change signal lead formed on the semiconductor chip, the context change signal lead carrying a signal having a first state indicating a context of a first set of program instructions operating on first data stored in the selected registers and a second state indicating a context of a second set of program instructions operating on second data stored in the selected registers", and "context switching circuitry formed on the semiconductor chip, the context switching circuitry being connected to the selected registers and the context change signal lead, the context change switching circuitry connecting one of the pair of first and second registers, for each selected register, to hold the first data in response to the first state of the context change signal and connecting the other of the pair of first and second registers, for each selected register, to hold the second data in response to the second state of the context change signal."*

The claimed differences would be obvious to an engineer of ordinary skill because the instant claims are merely embodiments of the claims recited in the previously patented invention, e.g., **independent claim 41 of the instant**

application claims:

A system comprising:

- A. a microphone having output leads;
- B. a speaker having input leads; and
- C. a processor including:
 - i. a semiconductor chip having microphone input leads connected to the microphone output leads and having speaker output leads connected to the speaker input leads;
 - ii. a processor formed on the chip and coupled to the microphone input leads and the speaker output leads, the processor including an ALU and selected registers that are associated with the ALU, each selected register being formed

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of a pair of first and second registers, the ALU storing program data in one of the first and second registers for each selected register;

iii. a context change signal lead formed on the semiconductor chip, the context change signal lead carrying a signal having a first state indicating a context of a first set of program instructions operating on first data stored in the selected registers and a second state indicating a context of a second set of program instructions operating on second data stored in the selected registers;

and

iv. context switching circuitry formed on the semiconductor chip, the context switching circuitry being connected to the selected registers and the context change signal lead, the context change switching circuitry connecting one of the pair of first and second registers, for each selected register, to hold the first data in response to the first state of the context change signal and connecting the other of the pair of first and second registers, for each selected register, to hold the second data in response to the second state of the context change signal.

as opposed to

A. a semiconductor chip;

B. a processor formed on the chip, the processor including an ALU and selected registers that are associated with the ALU, each selected register being formed of a pair of first and second registers, the ALU storing program data in one of the first and second registers for each selected register;

C. a context change signal lead formed on the semiconductor chip, the context change signal lead carrying a signal having a first state indicating a context of a first set of program instructions operating on first data stored in the selected registers and a second state indicating a context of a second set of program instructions operating on second data stored in the selected registers; and

D. context switching circuitry formed on the semiconductor chip, the context switching circuitry being connected to the selected registers and the context change signal lead, the context change switching circuitry connecting one of the pair of first and second registers, for each selected register, to hold the first data in response to the first state of the context change signal and connecting the other of the pair of first and second registers, for each selected register, to hold the second data in response to the second state of the context change signal

as claimed in independent claim 1 of the previously patented invention.

Because the instant claims are mere variations/additions on the limitations from

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the set of elements and functions claimed in the previously patented invention, such modifications would be readily apparent to an engineer of ordinary skill.

Terminal Disclaimer

3. A timely filed terminal disclaimer in compliance with 37 C.F.R. ' 1.321(b) would overcome an actual or provisional rejection on this ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 C.F.R. ' 1.78(d).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. The U.S. Patents used in the art rejections below have been provided as text documents which correspond to the U.S. Patents. The relevant portions of the text documents are cited according to page and line numbers in the art rejections below. For the convenience of Applicant, the cited sections are highlighted in the *text documents*. Consistent with Office procedure, the U.S. Patents corresponding to the *text documents* are also included with this action.

5. Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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6. Claims 41 and 43-44 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Berenbaum (U.S. Patent 4,484,274) in view of Pinede et al. (U.S. Patent 4,554,413).

As to claims 41 and 43-44, Berenbaum teaches a semiconductor chip (p3 26-49) a processor formed on the chip including an ALU (microprocessor is operative to execute operations in ALU 30, p4 23-31) and selected registers that are associated with the ALU (registers in 1 and 2 of table I, p2 19-40), each selected register formed of first and second *registers (registers 1 and 2 in table I)* a context change signal (R-bit, p6 39-55), and context switching circuitry connecting one of the first or second registers depending on the context switch signal (general purpose registers are connected depending on R-bit, p5 6-20). Berenbaum does not explicitly disclose the additional limitations detailed below.

Pinede teaches "microprocessor 502 is connected to the audio circuitry of the telephone" p8 45-49, which corresponds to the semiconductor chip having connections to/from the microphone and speaker.

It would have been obvious to combine Pinede's teachings with Berenbaum because the context switching could be implemented with Pinede's telephone I/O functions for data and full duplex communications through integrating the context switching microprocessor component in the telephone device.

7. Claims 42, 45 and 48-51 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Berenbaum and Pinede as applied to claim 41 and further in view of Gill et al. (U.S. Patent 4,916,651).

As to claims 42, 45 and 48-51, recognizing that the particular registers used in a system would depend on the application, then it follows from Gill's teachings to show a floating point processor which contains multiplexers to choose between registers (32,34), multiplier 48, ALU 54 and registers operating on clock edges see fig. 1. It would have been obvious to one of ordinary skill in the art to use the particular elements recited in the claims so that a floating point processor could be implemented in the Berenbaum/pinede system.

8. Claims 46-47 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Berenbaum and Pinede as applied to claim 41 and further in view of Namimoto et al. (U.S. Patent 4,217,638).

As to claims 46-47, Namimoto (fig. 6) further teaches context switch circuitry changing the flow of data being received from the first register to the second register. It would have been obvious to combine Namimoto's switching between register sets with Berenbaum as modified because it would provide faster context switching.

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9. The prior art of record and not relied upon is considered pertinent to the applicant's disclosure. Specifically, the below reference(s) will also have relevancy to one or more elements of the Applicant's claimed invention as follows:

U.S. Patent No. 5,021,993 to Motoba et al. which teaches the context switching for multiple program/task execution; and,

U.S. Patent No. 4,551,832 to Carll et al. which teaches the microprocessor control mechanisms in process management of audio devices.

10. Contact Information:

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system.

Status information for published applications may be obtained from either Private-PAIR or Public-PAIR.

Status information for unpublished applications is available through Private-PAIR only.

For more information about the PAIR system, see
<http://pair-direct.uspto.gov>.

Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

- ☐ All responses sent by U.S. Mail should be mailed to:

**Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450**

- ☐ Hand-delivered responses should be brought to Crystal Park Two, 2021 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist). All hand-delivered responses will be handled and entered by the docketing personnel. Please do not hand deliver responses directly to the Examiner.

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The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

All OFFICIAL faxes will be handled and entered by the docketing personnel. The date of entry will correspond to the actual FAX reception date unless that date is a Saturday, Sunday, or a Federal Holiday within the District of Columbia, in which case the official date of receipt will be the next business day. The application file will be promptly forwarded to the Examiner unless the application file must be sent to another area of the Office, e.g., Finance Division for fee charging, etc.

- ☐ Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist at **(703) 305-9600**.
- ☐ Any inquiry concerning this communication or earlier communications from the examiner should be directed to George Opie at (703) 308-9120 or via e-mail at *George.Opie@uspto.gov*. Internet e-mail should not be used where sensitive data will be exchanged or where there exists a possibility that sensitive data could be identified unless there is an express waiver of the confidentiality requirements under 35 U.S.C. 122 by the Applicant. Sensitive data includes confidential information related to patent applications.



MENG-AL T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100